REMARKS

Claims 1-54 are pending in the application. Claim 51 is objected to because of dependency. Claims 1-54 are rejected under 35 U.S.C. 103(a). Of the claims, claims 1, 18, 35, 52 and 53 are independent. The application, as argued herein, is believed to overcome the rejections.

Regarding Objections to the Claims

Claim 51 has been objected to because the Examiner believes that it should depend on claim 50 instead of claim 18. In response, claim 51 has been amended to depend on claim 50. Removal of the objection to claim 51 is respectfully respected.

Regarding Rejections under 35 U.S.C. 103(a)

To establish a prima facie case for obviousness under 35 U.S.C. § 103 (a), (1) there must be some suggestion or motivation to combine reference teachings. (2) There must be a reasonable expectation of success. (3) The references when combined must teach or suggest all the claim limitations. For the reasons discussed below, it is respectfully submitted that the Office has not established a prima facie case under 35 U.S.C. § 103 (a) for claims 1-54, and that therefore, claims 1-54 are allowable.

Claims 1-12, 15, 18-29, 32, 35-46, 49, 52 and 53-54 are rejected under 35 U.S.C. § 103 (a) as being deemed unpatentable over U.S. Patent No. 6,519,498 (Jevtic) in view of U.S. Patent Application No. 2001/0042189 (Babaian). Claims 13, 14, 16, 17, 30, 31, 34, 47, 48, 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jevtic in view of Babaian as applied to claims 1, 15, 18, 32, 35 and 49 above, in view of U.S. Patent No. 6, 178,542 (Dave).

The Applicants' claimed invention is directed to a computer implemented scheduling method for assigning tasks in a constrained dynamic application program to processors; that is, scheduling tasks in an application program while the application program is executing in a computer. A set of static schedules is defined for the application program based on scheduling states. Each static schedule includes an assignment of tasks in the application program to processors. During run time, a cost of a set of static schedules based on performance of the

application program is learned and a static schedule with a lowest cost is designated as an optimal schedule for a scheduling state. (*See* Page 8, lines 1-3, Page 5, lines 18-19 in the Applicants' specification as originally filed.)

Cited prior art, Jevtic is directed to analyzing schedules for a multi-cluster tool that is used for semiconductor wafer processing. Prior to run time, all possible schedules are generated and analyzed to determine a schedule that produces the highest throughput in the multi-cluster tool. The schedule with the highest throughput is deemed optimal and is downloaded to the sequencer in the multi-cluster tool. (*See* Col. 14, lines 57-64.)

Cited prior art, Babaian is directed to a compiler that divides a computer program into a plurality of streams of processor instructions to allow a wide instruction (combination of the streams) to be executed in parallel on a plurality of processors. Execution time of the program is reduced by processing multiple instructions in parallel on different processors, with the number of streams of instructions being equal to the number of processors. (*See* Page 1, [0011].)

Cited prior art Dave is directed to deriving the architecture of an embedded system from a task graph using hardware-software co-synthesis (simultaneous synthesis of the hardware and software architectures). Dave discusses use of a task graph to derive an architecture for an embedded system. (*See* Col. 13, lines 40-66; Col. 4, lines 17-20 and Abstract.)

In contrast to the cited prior art, the Applicants' disclosed invention is directed to an application program. (*See* Fig. 13, 408, 420.) Cited prior art Jevtic merely discusses a manufacturing process such as wafer processing and photolithography that are used in manufacturing of semiconductors, these processes are commonly referred to as "manufacturing applications". The claims have been amended to more clearly define that the Applicants' claimed application is an "application program" and the tasks that are assigned to processors are "tasks in the application program". (*See* Page 25, lines 8-14 in the applicants' application as originally filed.)

Jevtic merely discusses selecting an optimal schedule for semiconductor wafer processing (manufacturing process (application)) by analyzing scheduling algorithms using a main routine that is stored in memory in a computer system and executed by a single microprocessor in the computer system. The microprocessor executes the main routine to determine an optimum schedule for a multi-cluster tool. (*See* Fig. 2, 300 (main routine); 204 (memory); 202

(microprocessor); 200 (computer system); 212 (scheduling algorithms); and Col. 5, lines 50-52.) The main routine is only executed prior to run-time to analyze scheduling algorithms and the optimal scheduling algorithm is selected based on the results. Thus, Jevtic does not teach the applicants' claimed "during run-time, learning a cost of a set of static schedules" because only an optimal scheduling algorithm is selected and downloaded to multi-chamber tool prior to starting the manufacturing process. Furthermore, Jevtic does not even suggest "an assignment of tasks in the application program to processors" because Jevtic merely discusses a system having a single microprocessor.

Babaian's discussion of executing a plurality of instructions in a program in parallel on a plurality of processors does not teach or suggest the Applicants' claimed "assignment of tasks in the application to processors". There is no discussion of assigning tasks in the computer program to processors. Babaian merely describes instruction-level processing of a computer program and does not even suggest the Applicants' claimed "tasks in the computer program".

The dependent claims recite further limitations that are neither taught or suggested by the cited prior art. For example, Dave's discussion of dollar cost does not teach or suggest the Applicants' "predicting the cost of a schedule dependent on stored task execution costs" as claimed in claim 13. Dave's discussion of finish time estimation technique and example task graphs does not teach or suggest the Applicants' "schedule is selected for further exploration dependent on the predicted schedule cost" as claimed in claim 14.

Jevtic is directed to analyzing scheduling algorithms for a manufacturing process prior to starting the process. Babaian is directed to compiling instructions in a computer program prior to execution of the computer program and Dave is directed to synthesis of the hardware and software architectures. One of ordinary skill in the art of manufacturing processes would not look to compilers or to synthesis of hardware and software architectures. Thus, there is no suggestion or motivation to combine reference teachings. Even if combined, the present invention as now claimed does not result as argued above.

Claims 13, 14, 16, and 17 are dependent on Claim 1, Claims 30, 31, 33, and 34 are dependent on Claim 18, Claims 47, 48, 50 and 51 are dependent on Claim 35. Accordingly, these claims should be found in allowable condition for the same reasons as claim 1, 18 and 35 above, as well as on the basis of additional limitations in these claims.

Thus, none of the cited art alone or in combination teaches or suggests the applicants' claimed invention. Accordingly, the present invention as now claimed is not believed to be made obvious by the cited art or any of the prior art. In view of the foregoing, reconsideration of the rejections under 35 U.S.C. § 103(a) is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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